Parallel Processing

By

Fahad Layth Malallah

2-Architecture Classification

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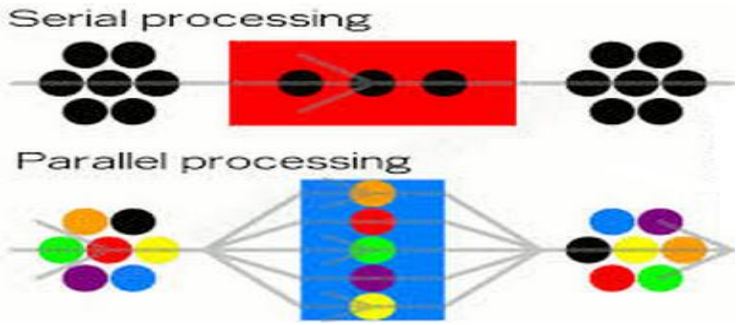


Reference Books:

1- F. B. Moreshwer, **Parallel Computing**, Addison-Wesley Publishing Company, 2008.
2- M. Morris Mano, **Computer System Architecture** ,3rd edition.
3-Hesham El-Rewini, Mostafa Abd-El-Barr, **Advanced Computer Architecture And Parallel Processing**, Weily, 2005.
4- David A. Patterson, Hohn L. Hinnessy, **Computer Organization and design: the hardware / Software interface**. 3rd edition, Elsevier, 2005.

Syllabus:

2. Architecture Classifications:

2.1- Flynn's Classification:

-SISD, SIMS, MISD, MIMD.

2.2- Shore's Classification.

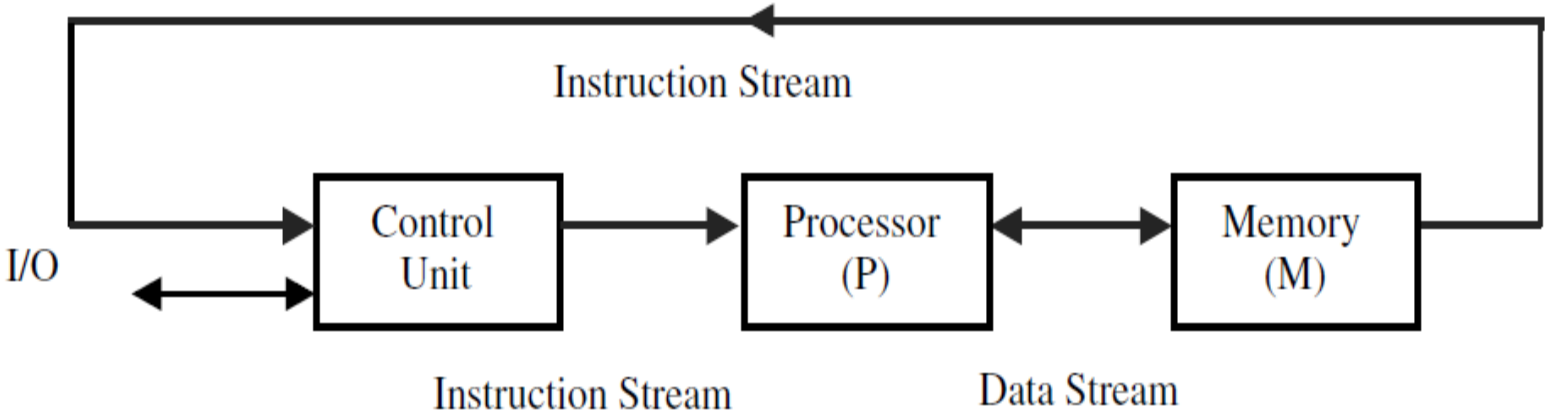
2.3- Feng's Classification.

2.4- Handler's Classification.

❑2.1- Flynn's Classification

1. SISD: Single Instruction Single Data.

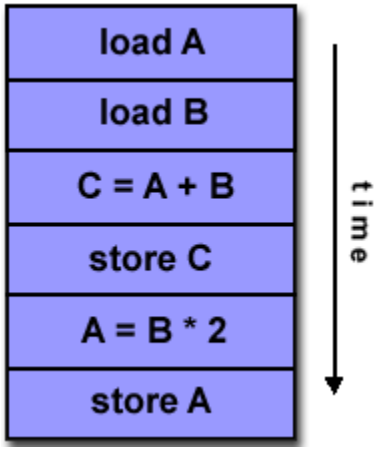
A- One Control Unit.
B- One Processing Unit.
C- One Memory unit.



❑2.1- Flynn's Classification

1. SISD: Single Instruction Single Data.

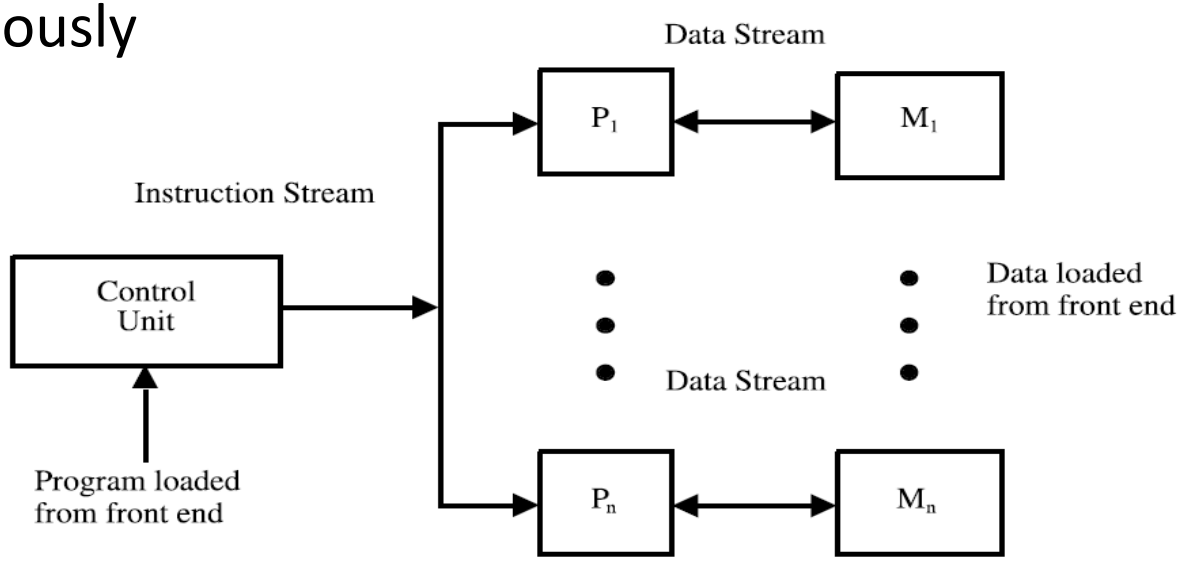
•A serial (non-parallel) computer
•Single instruction (SI): only one instruction stream is being acted on by the CPU during any one clock cycle.
•Single data (SD): only one data stream is being used as input during any one clock cycle.
•This is the oldest and until recently, the most prevalent form of computer.
•Examples: most PCs, single CPU workstations.



❑2.1- Flynn's Classification

2. SIMD: Single Instruction Multiple Data.

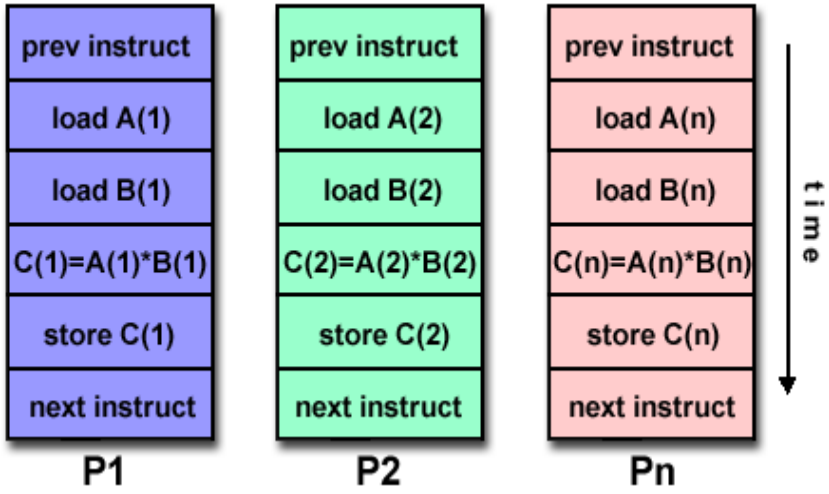
- Many processes unit under supervision of one control unit.
- All Processors (PE) receive same instruction from Control Unit (CU) but operate on different item of data.
- Memory must have ability to connect with all processors simultaneously



❑2.1- Flynn's Classification

2. SIMD: Single Instruction Multiple Data.

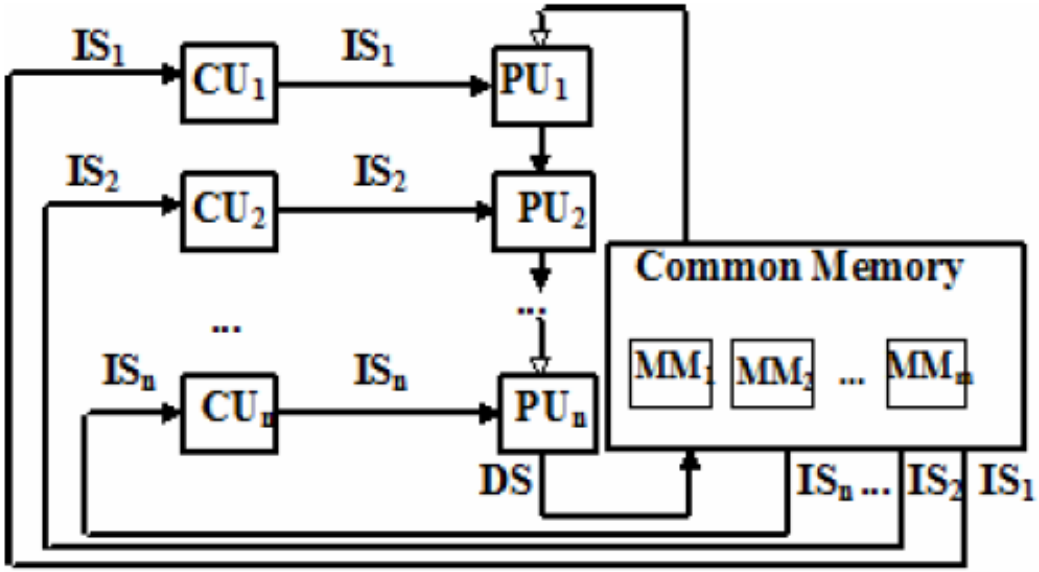
- A type of parallel computer.
- Single instruction: All processing units execute the same instruction at any given clock cycle.
- Multiple data: Each processing unit can operate on a different data element .
- Examples:
  - Vector Pipelines: IBM 9000, Cray C90, Fujitsu VP, NEC SX-2, Hitachi S820.



❑2.1- Flynn's Classification

2. MISD: Single Instruction Multiple Data.

- Multiple CU.
- Multiple PU.
- Data are taken from memory serially.
- All the PU execute the same single Datum.



❑2.1- Flynn's Classification

2. MISD: Single Instruction Multiple Data.

•A single data stream is fed into multiple processing units.

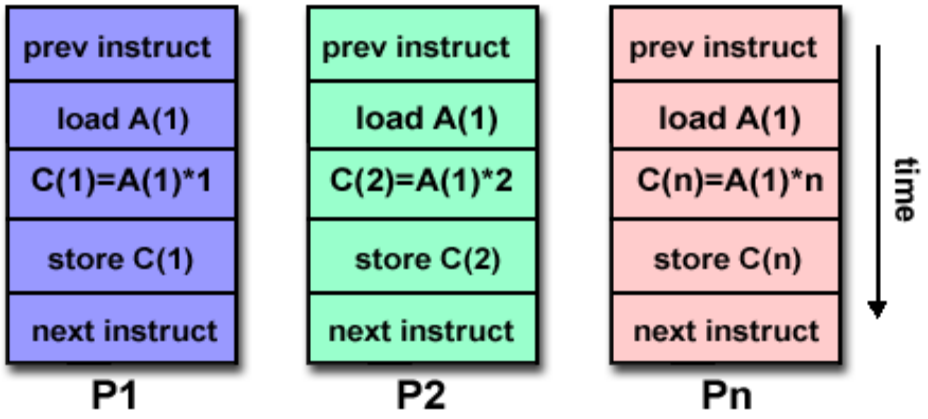
•Each processing unit operates on the data independently via independent instruction streams.

•Few examples of this class of parallel computer have ever existed, such as experimental Carnegie-Mellon C.mmp computer (1971).

•Some conceivable uses might be:

1-Multiple frequency **filters operating** on a single signal stream.

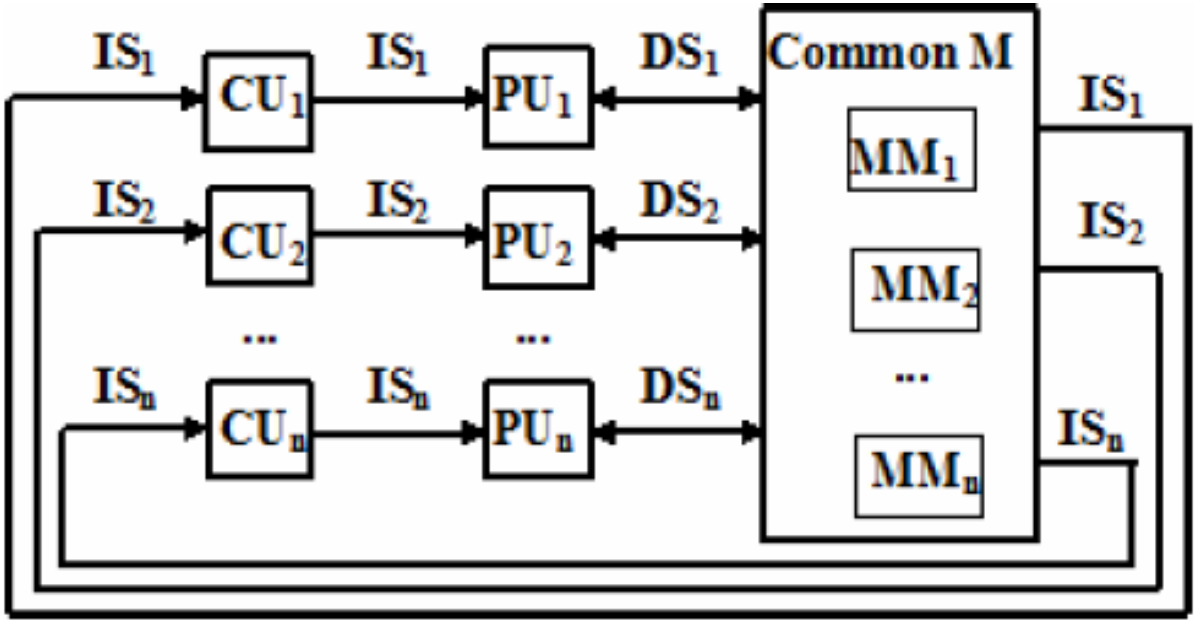
2-Multiple **cryptography** algorithms attempting to crack a single coded message.



❑2.1- Flynn's Classification

2. MIMD: Single Instruction Multiple Data.

- Multiple CU.
- Multiple PU.
- Different data are fetched into each CU and PU.
- Each PU executes different instruction.



❑2.1- Flynn's Classification

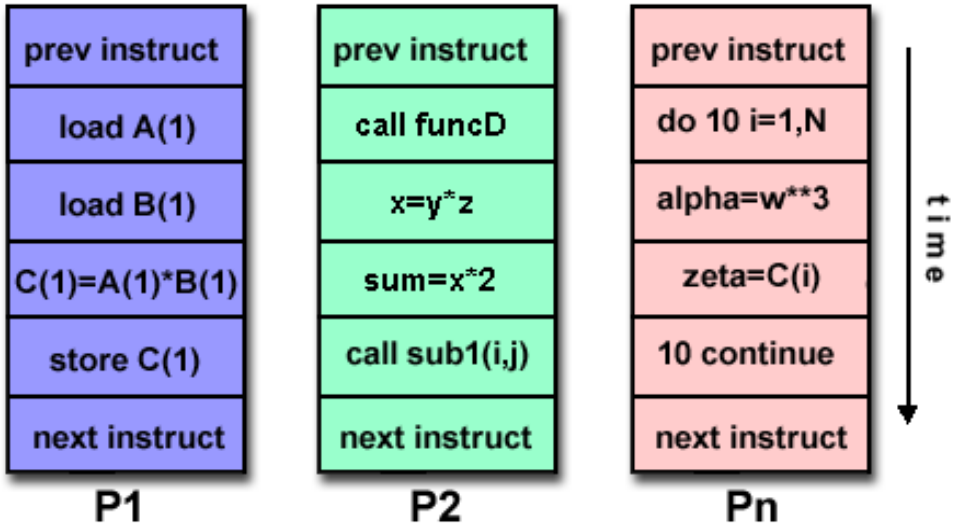
2. MIMD: Single Instruction Multiple Data.

•Currently, the most common type of parallel computer. Most modern computers fall into this category.

•Multiple Instruction: every processor may be executing a different instruction stream.

Multiple Data: every processor may be working with a different data stream .

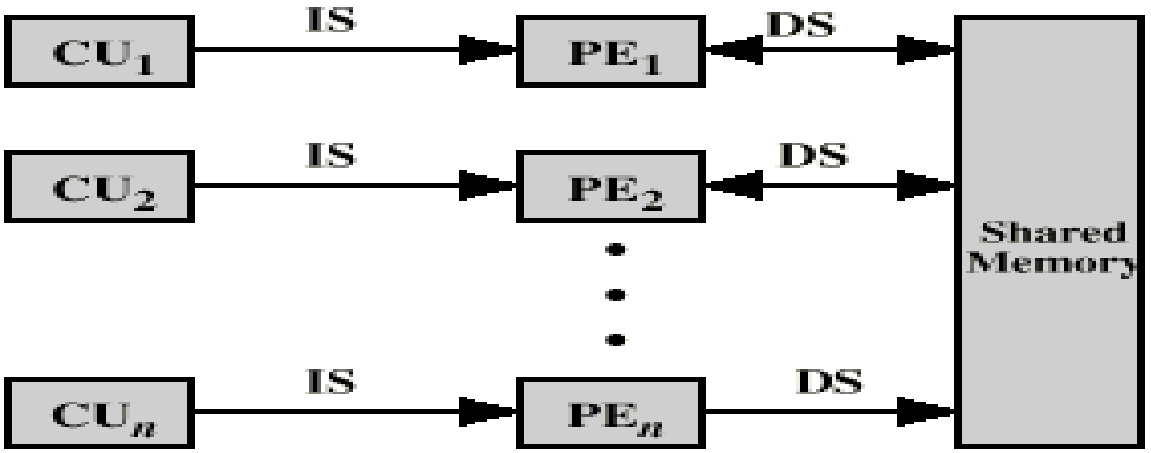
Examples: most current supercomputers, networked parallel computer "grids".



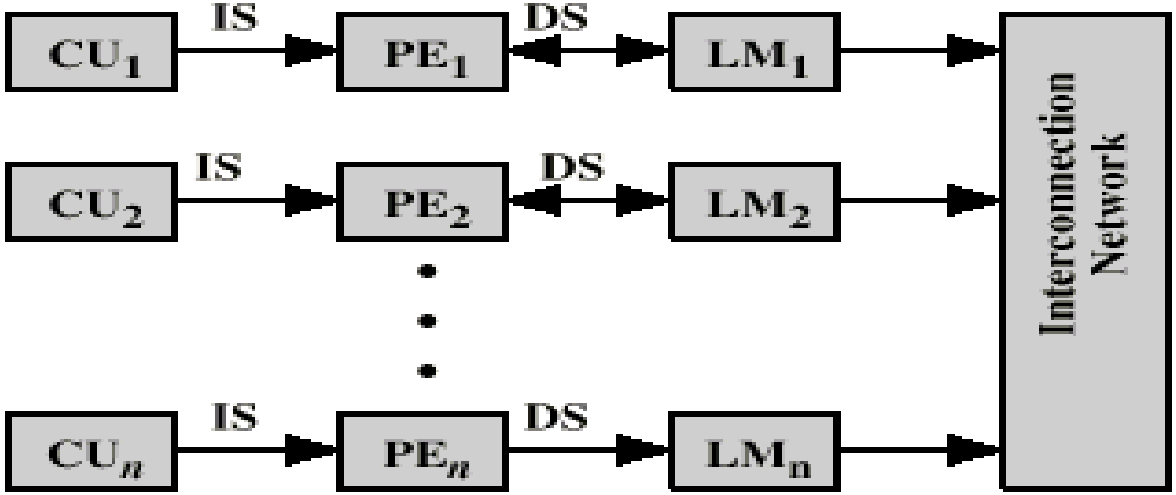
❑2.1- Flynn's Classification

2. MIMD: Single Instruction Multiple Data.

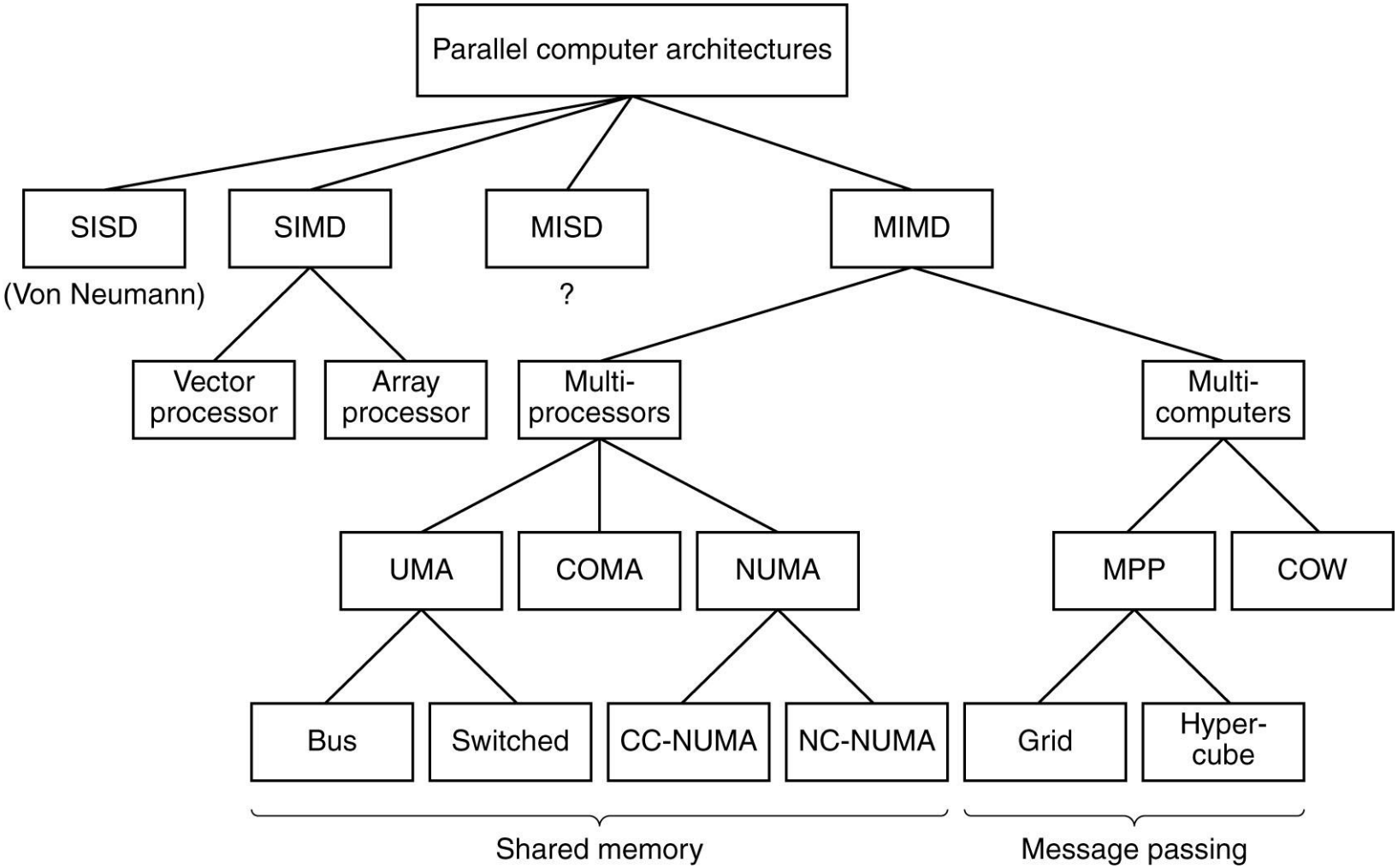
1-Share Memory.



2- Message Passing



❑2.1- Flynn's Classification



❑2.2- Shore's Classification.

•Classification is based on how the computer is organized from its **constituent parts**:

CU = Control Unit.

PU = Processing Unit.

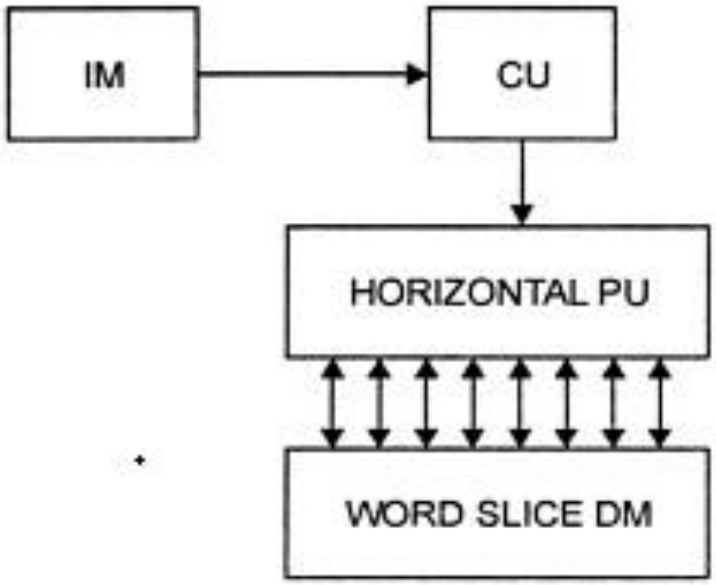
IM = Instruction Memory.

DM = Data Memory.

•Accordingly, 6-kind of machines were recognized by a designer:

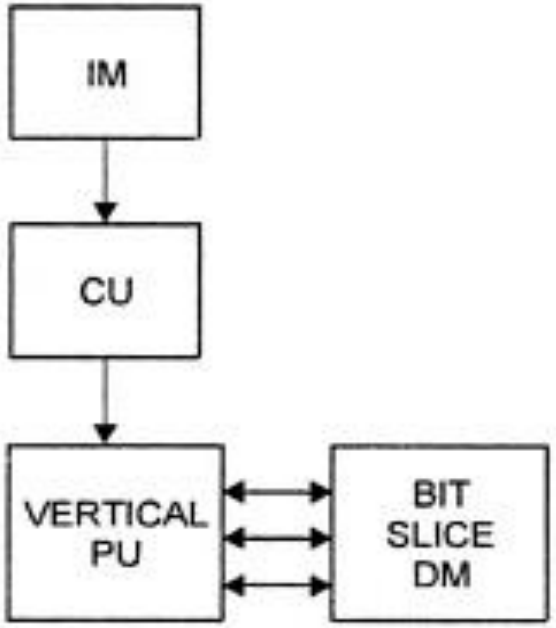
❑2.2- Shore's Classification.

Machine 1: has IM,CU, PU and DM. PU accesses the data horizontally (bit slice per single word memory.



(a) Machine 1

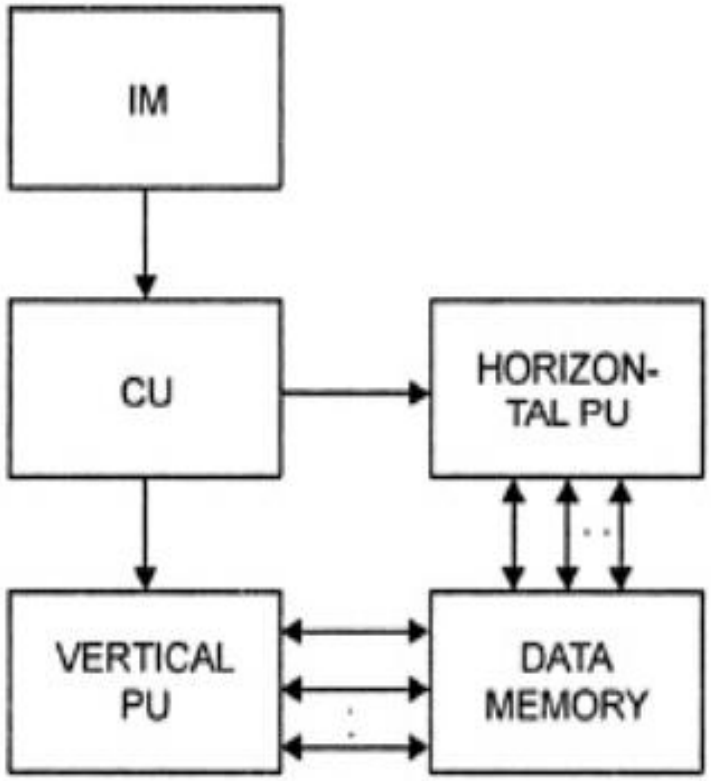
Machine 2: has IM,CU,PU and DM. PU accesses the data vertically (bit slice per multi-word memory).



(b) Machine 2

❑2.2- Shore's Classification.

•**Machine 3**: It is a combination of machine 1 and 2.
• It has IM,CU, PU and DM.
•PU Accessing the Data is done by both:
1-Horizontally: bit slice per single word memory.
2-Vertically: bit slice per mult-word memory.



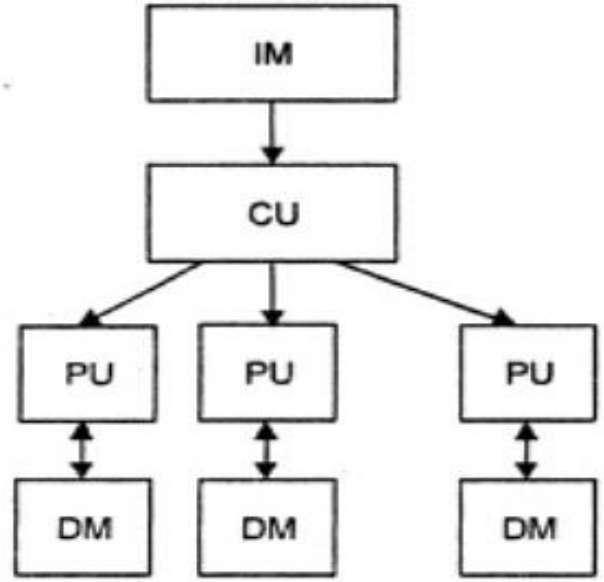
Machine 3

❑2.2- Shore's Classification.

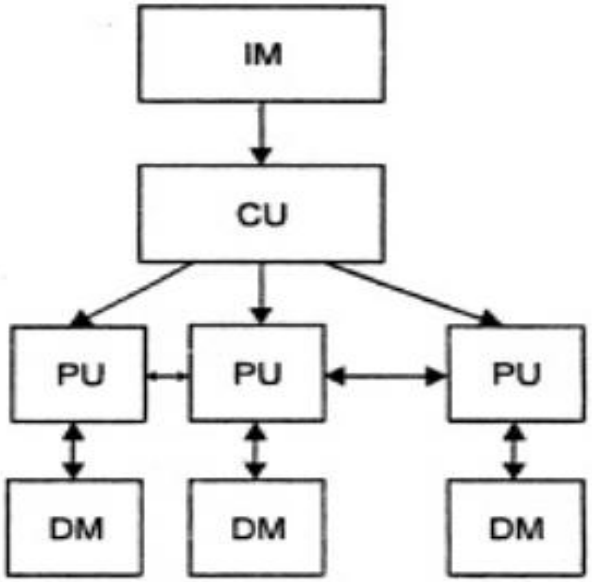
Machine 4: Multi-PU & DM under one CU. Without neighbor connection among PUs.

Machine 5: Multi PU & DM under one CU. With neighbor connection among PUs.

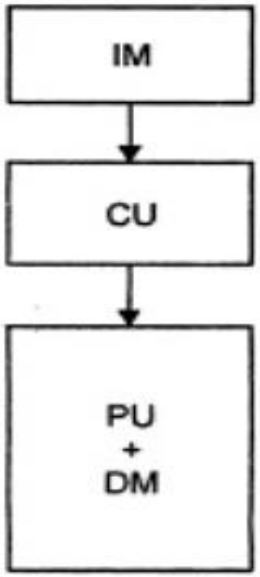
Machine 6: named Logic-in-memory array (LIMA**),** here , PU are distributed throughout the Memory.



(a) Machine 4



(b) Machine 5



(c) Machine 6

❑ 2.3- Feng's Classification.

•Tse-yun Feng suggested the use of **degree of parallelism** to classify various computer architectures.

•It is based on sequential and parallel operations at a **bit** and **word** level.

•There are 4 types of methods under above classification:

1- Word Serial and Bit Serial (WSBS)
2- Word Parallel and Bit Serial (WPBS)
3- Word Serial and Bit Parallel(WSBP)
4- Word Parallel and Bit Parallel (WPBP)

❑ 2.3- Feng's Classification.

•**WSBS:** has been called bit serial processing because one bit is processed at a time. (slow), example: (1,1).

•**WPBS:** has been called ***bit slice*** processing because m-bit slice is processes at a time. Example: (*,1).

•**WSBP**: ***Word Slice*** processing because one word of n-bit processed at a time. Example: (1,*).

•**WPBP:** is known as fully parallel processing in which an array on *n x m* bits is processes at one time. Example: (*,*).

It is failed with pipeline architecture.

❑ 2.4- Handler's Classification.

•It is an elaborate notation for expressing the pipelining and parallelism of computers. Handler's classification addresses the 3 distinct levels:

1- Processor Control Unit PCU → Processor.
2- Arithmetic Logic Unit ALU→ Functional unit and process element.
3- Bit-level Circuit(BLC) → Logic circuit needed to perform one bit operations in the ALU.

❑ 2.4- Handler's Classification.

•Handler's classification uses the following three pairs of integers to describe a computer:

Computer= (p*p', a* a', b*b').

p = Number of PCUs.
p' = Number of PCUs that can be pipelined.

a = Number of ALUs controlled by PCU.
a' = Number of ALUs that can be pipelined.

b = Number of bits in ALU or Processing element (PE) word.
b' = Number of Pipeline segments on all ALUs or in a single PE.

❑ 2.4- Handler's Classification.

Some notation for Handler's Classification :

- The '*' operator is used to indicate that the units are **pipelined** or macro-pipelined with a stream of data running through all the units.
- The '+' operator is used to indicate that the units are **not pipelined** but work on independent streams of data.
- The 'v' operator is used to indicate that the computer hardware can work in one of **several modes**.
- The '~' symbol is used to indicate a **range** of values for any one of the parameters.
- Peripheral processors are shown before the main processor using another three pairs.

❑ 2.4- Handler's Classification.

Example-1

Instrument's Advanced Scientific Computer (ASC) has one controller coordinating four arithmetic units. Each arithmetic unit is an eight stage pipeline with 64-bit words. Thus we have:

Answer: Handler's classification of ASC = (1, 4, 64 * 8)

Example-2

The Cray-1 is a 64-bit single processor computer whose ALU has twelve functional units, eight of which can be chained together to from a pipeline. Different functional units have from 1 to 14 segments, which can also be pipelined. Handler's description of the Cray-1 is:

Answer: Handler's classification of Cray-1 = (1, 12 * 8, 64 * (1 ~ 14))

❑ Summary

Architecture Classifications:

1. Flynn's Classification: based on Information (Instruction & Data) stream, has four types: SISD, SIMS, MISD, MIMD.

2. Shore's Classification: based on the computer constituent parts, it has 6 types.

3. Feng's Classification: based on the degree of the parallelism, it has 4 types: WSBS, WSBP, WPBS, WPBP.

4. Handler's Classification: based on a specific expression that describes the computer parts.

❑Exercises

1- According to Flynn's Taxonomy, write a simple program show the branches.

2- According to Flynn's Taxonomy, draw a diagram depicting MISM.

3- Flynn Classification is based on _____ , while Shores 'one is based on _____ .

4- Explain Feng's classification briefly?.

5- Multi-core or mult-processor, under which branch of flynn 's classification.

6- Explain and draw all shores 's classification?.

❑Exercises

7- The CDC 6600 has a single main processor supported by 10 I/O processors. One control unit coordinates one ALU with a 60-bit word length. The ALU has 10 functional units which can be formed into a pipeline. The 10 peripheral I/O processors may work in parallel with each other and with the CPU. Each I/O processor contains one 12-bit ALU. What is the handler's classification for both:

1- CDC 6600 Main Processor.

2- CDC 6600 I/O processor.

3- Overall the system of CDC 6600.